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WHAT IS CLAIMED IS:

1. A logic circuit, comprising:
2 a first inversion section for inverting a first
3 input signal having one of positive logic and negative
4 logic and outputting the inverted signal;
5 a second inversion section for inverting a second
6 input signal having the other of the positive logic and
7 the negative logic and outputting the inverted signal;
8 and
9 a transmission section for selectively outputting
10 one of the output of said first inversion section and the
11 output of said second inversion section in accordance with
12 a logical value which depends upon an externally
13 controllable selection signal and an inverted signal of
14 the selection signal.

1. 2. A logic circuit, comprising:
2 a first inversion section for inverting a first
3 input signal and outputting the inverted signal;
4 a second inversion section for inverting a second
5 input signal and outputting the inverted signal;
6 a first outputting section for selectively
7 outputting one of the output of said first inversion
8 section and the output of said second inversion section
9 in accordance with a logical value which depends upon an
10 externally controllable first selection signal and an
11 inverted signal of the first selection signal; and
12 a second outputting section for selectively

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13 ~outputting one of the output of said first inversion
14 section and the output of said second inversion section
15 in accordance with a logical value which depends upon an
16 externally controllable second selection signal and an
17 inverted signal of the second selection signal.

1 3. A logic circuit, comprising:
2 a first inversion section for inverting a first
3 input signal and outputting the inverted signal;
4 a second inversion section for inverting a second
5 input signal and outputting the inverted signal; and
6 a transmission section capable of discriminating
7 a magnitude relationship of 1 bit between the first input
8 signal and the second input signal and outputting a result
9 of the discrimination using a plurality of status signals.

1 4. The logic circuit according to claim 3, wherein said
2 transmission section includes a first gate section for
3 indicating whether or not the first input signal is equal
4 to or greater than the second input signal, a second gate
5 section for indicating whether or not the first input
6 signal is greater than the second input signal, a third
7 gate section for indicating whether or not the first input
8 signal is equal to or smaller than the second input signal,
9 and a fourth gate section for indicating whether or not
10 the first input signal is smaller than the second input
11 signal.

1 5. A logic circuit, comprising:

2 a first comparison section for receiving a first

3 input signal of n_1 bits and a second input signal of n_1

4 bits, performing magnitude comparison between a

5 predetermined number of bits of the first input signal

6 and the predetermined number of bits of the second input

7 signal and outputting results of the comparison of the

8 predetermined number of bits as a p_1 th comparison result,

9 a p_2 th comparison result, a p_3 th comparison result and a

10 p_4 th comparison result using a plurality of status signals,

11 n_1 being an integer equal to 2 to the m_1 th power, m_1 being

12 an even number equal to or greater than 2;

13 a second comparison section for performing

14 magnitude comparison between a number of bits equal to

15 twice the predetermined number of bits of the first input

16 signal and a number of bits equal to twice the

17 predetermined number of bits of the second input signal

18 from the p_1 th comparison result and the p_2 th comparison

19 result and outputting a result of the comparison of the

20 predetermined number of bits as a p_5 th comparison result

21 using the plurality of status signals and for performing

22 magnitude comparison between a number of bits equal to

23 twice the predetermined number of bits of the first input

24 signal and a number of bits equal to twice the

25 predetermined number of bits of the second input signal

26 from the p_3 th comparison result and the p_4 th comparison

27 result and outputting a result of the comparison of the

28 predetermined number of bits as a p_6 th comparison result

29 using the plurality of status signals; and
30 a third comparison section for performing magnitude
31 comparison between the n_1 bits of the first input signal
32 and the n_1 bits of the second input signal from the p_5 th
33 comparison result and the p_6 th comparison result and
34 outputting a result of the comparison of the n_1 bits using
35 the plurality of status signals.

1 6. A logic circuit, comprising:
2 a half addition arithmetic section for receiving
3 a first input signal of n_2 bits and an inverted signal of
4 a second input signal of n_2 bits and performing half
5 addition arithmetic of the first input signal and the
6 inverted signal of the second input signal, n_2 being an
7 integer equal to 2 to the m_2 th power, m_2 being an even number
8 equal to or greater than 2;
9 a first arithmetic section for performing full
10 addition arithmetic of the first input signal and the
11 inverted signal of the second input signal separately for
12 each predetermined number of bits and outputting a result
13 of the full addition arithmetic as a q_1 th carry, a q_2 th
14 carry, a q_3 th carry and a q_4 th carry using a plurality of
15 status signals;
16 a second arithmetic section for outputting logical
17 AND information of the q_1 th carry and the q_2 th carry as
18 a q_5 th carry using the plurality of status signals and
19 outputting logical AND information of the q_3 th carry and
20 the q_4 th carry as a q_6 th carry using the plurality of status

21 signals;

22 a third arithmetic section for outputting logical

23 AND information of the carries of all of the n_2 bits as

24 a q_1 th carry using the plurality of status signals from

25 at least the q_5 th carry and the q_6 th carry; and

26 a fourth arithmetic section for performing logical

27 exclusive ORing of the output of said half addition

28 arithmetic section and the q_1 th carry and outputting a full

29 addition arithmetic result.

1. A logic circuit, comprising:

2 a first inversion section for inverting a first

3 input signal and outputting the inverted signal;

4 a second inversion section for inverting the

5 inverted signal of the first input signal and outputting

6 a resulting signal;

7 a first outputting section for performing NANDing

8 arithmetic between the output of said first inversion

9 section and a second input signal and outputting a

10 resulting signal; and

11 a second outputting section for performing NANDing

12 arithmetic between the output of said second inversion

13 section and an inverted signal of the second input signal

14 and outputting a resulting signal;

15 said first outputting section and said second

16 outputting section being switched with the second input

17 signal and the inverted signal of the second input signal.

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2 8. The logic circuit as claimed in claim 1, further comprising:

3 a first switching section provided on an input side
4 of said first inversion section and capable of performing
5 switching of whether the first input signal should be
6 passed or blocked in accordance with an external control
7 signal; and

8 a second switching section provided on an input side
9 of said second inversion section and capable of performing
10 switching of whether the second input signal should be
11 passed or blocked in accordance with the external control
12 signal.

1 9. A logic circuit, comprising:

2 a first carry generation section for receiving a
3 first input signal $A<0: n_3>$ of n_3 bits and an inverted
4 signal $XA<0:n_3>$ of the first input signal of n_3 bits and
5 outputting a first logical AND result and a first logical
6 AND inversion result as a logical AND result at least of
7 bits $A<0>$ to $A<2$ to the m_3 th power - 1 from the first input
8 signal bits $A<0: 2$ to the m_3 th power - 1 and the inverted
9 signal bits $XA<0: 2$ to the m_3 th power - 1, n_3 being an
10 integer equal to 2 to the m_3 th power, m_3 being an even number
11 equal to or greater than 2;

12 a second carry generation section for outputting
13 a second logical AND result and a second logical AND
14 inversion result as a logical AND result at least of bits

15 $A<2 \text{ to the } m_3 \text{th power}>$ to $A<2 \times 2 \text{ to the } m_3 \text{th power - 1}>$
16 from the first input signal bits $A<2 \text{ to the } m_3 \text{th power:}$
17 $2 \times 2 \text{ to the } m_3 \text{th power - 1}>$ and the inverted signal bits
18 $XA<2 \text{ to the } m_3 \text{th power: } 2 \times 2 \text{ to the } m_3 \text{th power - 1}>;$
19 a third carry generation section for outputting a
20 third logical AND result and a third logical AND inversion
21 result as a logical AND result at least of bits $A<2 \times 2$
22 to the $m_3 \text{th power}>$ to $A<3 \times 2 \text{ to the } m_3 \text{th power - 1}>$ from
23 the first input signal bits $A<2 \times 2 \text{ to the } m_3 \text{th power: } 3$
24 $\times 2 \text{ to the } m_3 \text{th power - 1}>$ and the inverted signal bits
25 $XA<2 \times 2 \text{ to the } m_3 \text{th power: } 3 \times 2 \text{ to the } m_3 \text{th power - 1}>;$
26 a fourth carry generation section for outputting
27 a fourth logical AND result and a fourth logical AND
28 inversion result as a logical AND result at least of bits
29 $A<3 \times 2 \text{ to the } m_3 \text{th power}>$ to $A<4 \times 2 \text{ to the } m_3 \text{th power}$
30 $- 1>$ from the first input signal bits $A<3 \times 2 \text{ to the } m_3 \text{th power}$
31 $: 4 \times 2 \text{ to the } m_3 \text{th power - 1}>$ and the inverted signal
32 bits $XA<3 \times 2 \text{ to the } m_3 \text{th power: } 4 \times 2 \text{ to the } m_3 \text{th power}$
33 $- 1>;$
34 a first logical AND generation section for receiving
35 the first logical AND result and the first logical AND
36 inversion result as well as the second logical AND result
37 and the second logical AND inversion result and outputting
38 a fifth logical AND result and a fifth logical AND
39 inversion result as a logical AND result at least of the
40 bits $A<0>$ to $A<2 \times 2 \text{ to the } m_3 \text{th power - 1}>;$
41 a second logical AND generation section for

42 receiving the third logical AND result and the third
43 logical AND inversion result as well as the fourth logical
44 AND result and the fourth logical AND inversion result
45 and outputting a sixth logical AND result and a sixth
46 logical AND inversion result as a logical AND result at
47 least of the bits A<2 × 2 to the m_3 th power> to A<4 × 2
48 to the m_3 th power - 1>;

49 a third logical AND generation section for
50 outputting a seventh logical AND result and a seventh
51 logical AND inversion section as a logical AND result at
52 least of the bits A<0> to A<2 × 2 to the m_3 th power - 1>
53 from the fifth logical AND result and the fifth logical
54 AND inversion result as well as the sixth logical AND
55 result and the sixth logical AND inversion result;

56 a fourth logical AND generation section for
57 outputting an eighth logical AND result and an eighth
58 logical AND inversion result as a logical AND result at
59 least of the bits A<2 to the m_3 th power> to A<3 × 2 to the
60 m_3 th power - 1> from the second logical AND result and the
61 second logical AND inversion result as well as the sixth
62 logical AND result and the sixth logical AND inversion
63 result; and

64 a full addition arithmetic section for outputting
65 a full addition arithmetic result of n_3 bits from a first
66 gate signal of n_3 bits which includes the seventh logical
67 AND result, the eighth logical AND result, the sixth
68 logical AND result and the fourth logical AND result and

69 a second gate signal of n_3 bits which includes the seventh
70 logical AND inversion result, the eighth logical AND
71 inversion result, the sixth logical AND inversion result
72 and the fourth logical AND result.

1 10. The logic circuit as claimed in claim 3, wherein
2 the plurality of status signals includes a first gate
3 signal for indicating whether or not the first input
4 signal is equal to or greater than the second input signal,
5 a second gate signal for indicating whether or not the
6 first input signal is greater than the second input signal,
7 a third gate signal for indicating whether or not the first
8 input signal is equal to or smaller than the second input
9 signal, and a fourth gate signal for indicating whether
10 or not the first input signal is smaller than the second
11 input signal.

1 11. The logic circuit as claimed in claim 5, wherein
2 the plurality of status signals includes a first gate
3 signal for indicating whether or not the first input
4 signal is equal to or greater than the second input signal,
5 a second gate signal for indicating whether or not the
6 first input signal is greater than the second input signal,
7 a third gate signal for indicating whether or not the first
8 input signal is equal to or smaller than the second input
9 signal, and a fourth gate signal for indicating whether
10 or not the first input signal is smaller than the second

11 ~~input signal.~~

1 12. The logic circuit as claimed in claim 6, wherein
2 the plurality of status signals includes a first gate
3 signal for indicating whether or not the first input
4 signal is equal to or greater than the second input signal,
5 a second gate signal for indicating whether or not the
6 first input signal is greater than the second input signal,
7 a third gate signal for indicating whether or not the first
8 input signal is equal to or smaller than the second input
9 signal, and a fourth gate signal for indicating whether
10 or not the first input signal is smaller than the second
11 input signal.

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